REMARKS

Claims 1, 3-12, 14-23, and 25-33 were pending in this application.

Claims 1, 3-5, 12, 14-16, 23, and 25-27 have been rejected.

Claims 6-11, 17-22, and 28-33 have been objected to.

Claims 1, 12, and 23 have been amended as shown above.

Claims 1, 3-12, 14-23, and 25-33 remain pending in this application.

Reconsideration and full allowance of Claims 1, 3-12, 14-23, and 25-33 are respectfully requested.

I. ALLOWABLE CLAIMS

The Applicants thank the Examiner for the indication that Claims 6-11, 17-22, and 28-33 would be allowable if rewritten in independent form to incorporate the elements of their respective base claims and any intervening claims. Because the Applicants believe that the remaining claims in this application are allowable, the Applicants have not rewritten Claims 6-11, 17-22, and 28-33 in independent form.

II. REJECTION UNDER 35 U.S.C. § 102

The Office Action rejects Claims 1, 3-5, 12, 14-16, 23, and 25-27 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,130,565 to Nagano et al. ("*Nagano*"). The Applicants respectfully traverse this rejection.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if

every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. (*MPEP § 2131; In re Bond, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990)*). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. (*MPEP § 2131; In re Donohue, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985)*).

Nagano recites a phase locked loop (PLL) that includes a phase difference comparison circuit 202, a charge pump circuit 102, a filter 304, and a voltage controlled oscillation circuit 402. (*Figure 18; Col. 23, Line 67 – Col. 24, Line 4*). The oscillation circuit 402 includes a control circuit 4020 and multiple delay circuits 40201-40233. (*Figure 19; Col. 24, Lines 32-35*). The output of the first delay circuit 40201 and the output of the last delay circuit 40233 are provided to the phase difference comparison circuit 202. (*Figure 19; Col. 27, Lines 2-9*). The phase difference comparison circuit 202 generates "up" or "down" currents based on a comparison of its two inputs. (*Col. 24, Lines 5-8*).

Claims 1, 12, and 23 have been amended to recite determining that a "clock edge has reached an output of [a] first delay cell and has not reached an output of [a] second delay cell in response to a next sequential clock edge being applied to [a] delay cell input."

Nagano simply recites that the phase difference comparison circuit 202 generates "up" and "down" currents using two inputs from two different delay circuits 40201-40233. The phase difference comparison circuit 202 does not use a second clock edge to determine whether a first clock edge appears at the outputs of two different delay circuits 40201-40233. Rather, the phase difference comparison circuit 202 simply receives two signals and determines a phase difference

between them. *Nagano* does not recite that the phase difference comparison circuit 202 determines whether one "clock edge" has reached the outputs of two different delay circuits 40201-40233 "in response to" a second "clock edge" being supplied to an input of the delay circuit 40201. As a result, *Nagano* fails to anticipate determining that a "clock edge" has reached an output of a first delay cell and has not reached an output of a second delay cell "in response to" a "next sequential clock edge being applied" to a delay cell input as recited in Claims 1, 12, and 23.

For these reasons, *Nagano* fails to anticipate the Applicants' invention as recited in Claims 1, 12, and 23 (and their dependent claims).

Accordingly, the Applicants respectfully request withdrawal of the § 102 rejection and full allowance of Claims 1, 3-5, 12, 14-16, 23, and 25-27.

III. CONCLUSION

The Applicants respectfully assert that all pending claims in this application are in condition for allowance and respectfully request full allowance of the claims.

SUMMARY

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@davismunck.com*.

The Applicants have included the appropriate fee to cover the cost of a Request for Continued Examination. The Commissioner is hereby authorized to charge any additional fees connected with this communication (including any extension of time fees) or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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